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INVESTIGATION AND DESIGN OF ELECTRONIC CIRCUITRY RELATED TO NOISE AND RADIATION EFFECTS FOR SOLID STATE DEVICES AND CIRCUITS

Northeastern University

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This technical report has been reviewed and approved for publication.

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This report details the design and operation of an infrared detector scanning system. Operation involves detector charging, photon illumination, parallel signal transfer and serial readout using a CCD shift register. It provides six signals in the necessary sequence, magnitude and phase to drive MOS-FET type loads, variable bias supplies, DVM monitoring and a digital word generator.

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1.0 Introduction

This report covers the design and fabrication of the electronic instrumentation required for a solid state multiple detector and CCD readout optical system. The detector scanning system consists of two packages, the Infra Red Detector Scanning System, IRDSS Model I, and the IR Det. IA Aux. Unit. The IRDSS Model I is a clocked three phase MOS-FET gated system capable of supplying five output signals in a prescribed sequential format. The IR Det. IA Aux. Unit consists of a digital word generator for electronic evaluation of the CCD shift registers, a voltage monitor with eight variable bias supplies and a reset pulse required for correct operation of the output of the CCD units.

1.1 Basic Requirements

The IR detectors, Schottky diodes, are momentarily charged in parallel while isolated from their individual CCD input wells. This charge voltage pulse will be referred to as Setting Pulse or S. The detectors then are illuminated while completely isolated. After this "staring time", referred to subsequently as integration time, the signal from each detector must be transferred to the input of a three well CCD unit, one unit for each detector. After signal transfer each detector must be isolated from the charging circuit and the input CCD well during the serial readout of the CCD shift register and prior to the subsequent charge interval. This control circuitry will be described later in Section 2.2 concerned with Sequence Control.

The physical structure of the CCD units under consideration required three phase operation in conjunction with a master clock. The master clock was to be free running at a nominal frequency of 1 MHz with the PRF and

Duty Cycle relatively independent of each other. Synchronization of the master clock with the three phase gate signals was not required by virtue of the synchronization afforded by the sequential control circuitry, as will be seen in later sections.

The physical structure of the CCD units also required that the three phase gate voltages overlap. This requirement was met with what will be referred to as gate expander or pulse stretcher circuits.

Thus, the five output signals referred to for the IRDSS Model I, are the Setting Gate signal, referred to as S or its complement $\overline{S}$, the Synchronized Transfer Pulse, STP or its complement $\overline{STP}$, and the three stretched phase pulses referred to as $\phi_1(s)$, $\phi_2(s)$ and $\phi_3(s)$. All five of these gate voltages were to be variable between 0 and 20 volts. Isolation of the detectors also required that the S and STP gates have the capability of negative off-set bias.

The reset gate voltage of the IR Det. IA Aux. Unit did not require an offset bias, but otherwise must meet the same requirements of the three phase gate voltages. The digital word generator output was set at 0 to 3 volts with an offset adjustable from 0 to 4 volts.

One final requirement was that the electronic system was to be flexible, with adequate test points and capable of being modified readily. A block diagram of the overall system is given in Figure 1.

1.2 Organization

In the interest of flexibility the physical system for the IRDSS Model I consists of five plug-in modules in a standard rack-mounting cage. The five modules are numbered and labelled as follows:

Panel 1	Master Clock
Panel 2	Sequence Control
Panel 3	Clock-Gate, Three Phase Generator
Panel 4	Gate Expander - Gate Driver
Panel 5	Power

The IR Det. IA Aux. Unit consists of three plug-in modules numbered and labelled as follows:

Panel 6	Digital Word Generator
Panel 7	Voltage Monitor
Panel 8	Bias Control

Details of the circuits for these panels will be discussed in subsequent sections.

2.1 Master Clock - Panel 1

The Master Clock circuit is an astable multivibrator circuit composed of two monostable IC's, SN74123, feeding back on one another. See Figure 2. The output pulse width of each of the monostable circuits is determined by a single RC combination. For this application a variable resistance, common to both units, in conjunction with individual C's, controls the duty cycle. A second variable resistance in series with V_{CC} and the duty cycle variable resistance controls the frequency or PRF. Interaction between these two variables was relatively insignificant.

The desired output from the Master Clock, Q or $\overline{Q}$, may be selected by a switch located on the front panel. Isolated clock pulses for the pulse stretcher circuits and the clock gating circuitry were made available by means of two inverters of the hex inverter SN7404.

2.2 Sequence Control - Panel 2

The Sequence Control circuitry consists of three monostable multivibrators in cascade using two SN74123's as indicated in Figure 3. In the subsequent discussion these monostable units will be referred to as FF_1, FF_2 and FF_3. FF_1 generates the S and $\overline{S}$ time interval. The $\overline{S}$ output is the input to the second monostable circuit, or FF_2. "Staring time", or integration time is determined by FF_2 and its associated timeconstant. FF_3 is triggered by the output of FF_2 and generates the Initial Transfer Pulse, ITP.

Provisions have been made for three possible inputs to the Sequence Control Circuitry. A front panel switch selects these as EXT, FTP or INT. The input EXT is a special input for a synchronizing signal from a light shutter. Such a signal is processed internally by two operational amplifiers which provide for both phase and magnitude control of the input synchronizing signal.

The FTP input is also an external input, however, it provides a means of synchronization by means of any signal source having the capability of triggering FF_1.

The INT input synchronizes the Sequence Control Circuitry by means of an internal astable multivibrator circuit utilizing an NE555 timer. Supply voltage for the NE555 circuit is removed on the other two input switch positions to avoid interaction. The PRF of the NE555 circuitry is controllable from the front panel with the INT PRF control. The pulse width is fixed at 1 millisecond and the PRF is variable from 10 to 100 HZ.

2.3 Clock Gate, Three Phase Generator - Panel 3

A working diagram of the Clock Gate and Three Phase Generator circuitry is shown in Figure 4. The Clock Gate circuitry consists of a dual D type flip-flop, SN7474, an AND gate, a Delay consisting of four buffer amplifiers in cascade, four units of an SN7407 Hex Buffer, and an output OR gate. The Three Phase Generator circuit consists of a dual JK Master-Slave Flip-Flop, SN7473, and a NOR gate, one gate of the SN7432 Quad Nor Gate.

Prior to an input ITP to the D_1 flip-flop there is no output from either D type flip-flops or the Delay. Consequently, the output from the OR gate to the Three Phase Generator is the Master Clock signal, and the CK signals for each JK unit is synchronized with the Master Clock. This applies as long as the ITP signal is low, or there is no output from the Delay into the OR gate.

Operation of the Three Phase Generator can be explained by means of the JK truth table and the interconnections of the two JK flip-flops. Note in Figure 4 that J_1 and Q_2 are common and Q_1 and J_2 are common. $K_1 = K_2 =$ 5 volts, or both are maintained at a logic level of 1. This means that only the bottom two conditions of the truth table in Figure 5 apply to the Three Phase generator circuit.

JK flip-flops operate only on the *fall* of the CK signal. Thus, from the truth table if J = K = 1 prior to the fall of the CK signal, then after the fall of the CK signal the output of the JK flip-flop will be inverted from its level prior to the CK signal. If J = 0 and K = 1 prior to the fall of the CK signal, then the output goes to 0 after the fall of the next CK signal.

Using the truth table of Figure 8 one can construct a table of logic levels for J_1, Q_1, etc. which will demonstrate the generation of two of the three phase pulses, ϕ_2 and ϕ_3. This program is shown below and starts at line one with the CK high and the *assumed* initial logic levels. Each fall of the clock is shown as ↓ and each succeeding line gives the logic levels after the fall of the clock.

Three Phase Generator Program

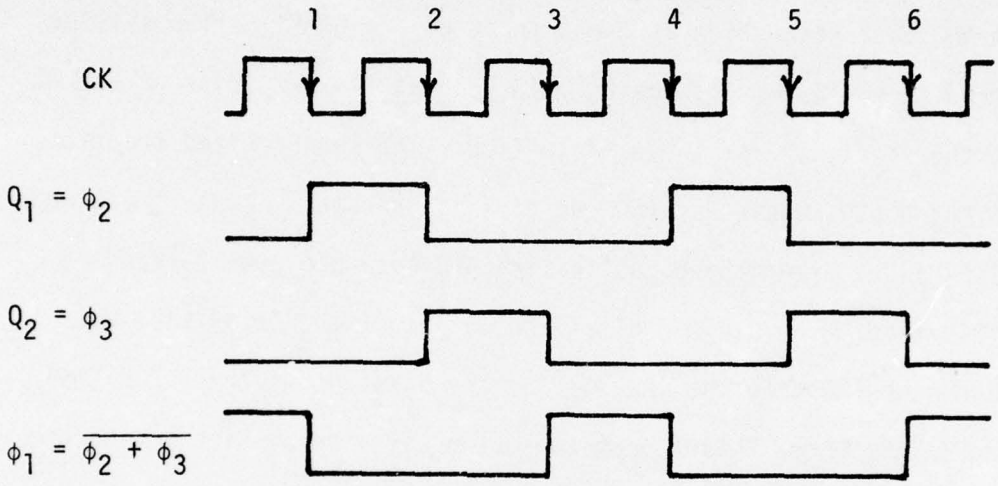
	ϕ_2			ϕ_3				
	J_1	K_1	Q_1	J_2	K_2	Q_2	$\overline{Q}_2$	CK
Logic levels prior to first fall of CK	1	1	0	0	1	0	1	
	1	1	1	1	1	0	1	↓1
	0	1	0	0	1	1	0	↓2
	1	1	0	0	1	0	1	↓3
	1	1	1	1	1	0	1	↓4
	0	1	0	0	1	1	0	↓5

After the first fall of CK, Q_1 has gone to the 1 level with Q_2 unchanged, or still at the 0 level. After the second fall of CK, Q_1 is at the 0 level and Q_2 has gone to the 1 level. After the third fall of CK both Q_1 and Q_2 are at the 0 level. Since $Q_1 = \phi_2$ and $Q_2 = \phi_3$, it can be seen that starting from the given assumptions ϕ_2 and ϕ_3 have been generated at the desired interval and phase.

ϕ_1 is generated at the output of the NOR gate. The NOR gate will go to the 1 level only when both inputs are at the 0 level. Otherwise the output remains at the 0 level, or, if at the 1 level, returns to the 0 level if either input is at the 1 level.

Note that after the third fall of CK both inputs to the NOR gate are low giving a high output. After the fourth fall of CK, Q_1 goes to a 1 level with Q_2 remaining at the 0 level and the output of the NOR gate returns to the 0 level. Thus, during the third and fourth fall of CK, during the interval when ϕ_2 and ϕ_3 are both at a 0 level, ϕ_1 is generated.

These results are demonstrated in a timing diagram shown below.



Timing diagram for Three Phase Generator

This discussion is valid only as long as there is only the MC signal at the input to the OR gate of the Clock Gate circuit. If a constant level of 1 is maintained at either input of the OR gate, the Three Phase Generator will be inoperative. Thus, it is possible for the Three Phase Generator to be turned off for the duration of the STP signal at the output of the Delay circuit. This capability is necessary since during the transfer of data to the CCD array, the synchronized transfer time, CCD readout should not occur.

Now assume that the Sequence Control circuitry initiates the FTP signal at the D input to the D_1 flip-flop and one input of the AND gate.

The other input of the AND gate Q_1 of the D_1 flip-flop. The D_1 input is transferred to Q_1 only on the next rise of $\overline{\phi}_3$, the CK signal for the D_1 flip-flop. Thus, the output from the AND gate will be delayed for the interval between the initiation of the input ITP and the next rise of $\overline{\phi}_3$ and ϕ_1.

The AND gate going high at the D input of the D_2 flip-flop will be transferred to the output of the D_2 flip-flop at the next rise of the MC which is the CK signal for the D_2 flip-flop. The synchronized transfer pulse, STP and $\overline{\text{STP}}$, begins at the end of this transfer. Thus, the start of the STP occurs after the output of the AND gate has been delayed by the D_2 flip-flop. The STP signal at the output of the Delay will now maintain a high input to the OR gate for the duration of the STP signal resulting in the Three Phase Generator being off with ϕ_1 high and ϕ_2 and ϕ_3 being low.

At the end of the ITP signal the AND gate terminates the D signal of the D_2 flip-flop immediately. On the next rise of the MC the 0 level of the D input is transferred to the output of the D_2 flip-flop terminating the STP and $\overline{\text{STP}}$ signals. The STP signal at the output of the Delay is terminated after a short delay determined by the characteristics of four buffer amplifiers in cascade. At the next fall of the MC the Three Phase Generator is again operative.

The Delay circuit is not crucial. It insures that the output of the OR gate does not go to zero at the end of the STP while the MC signal is low. It does not affect the operation at the beginning of the STP since ϕ_1 is already high, or at the 1 level.

A scope synch signal is available as the output of a unity gain operational amplifier. The amplitude is variable and may be referenced to either STP or $\overline{\text{STP}}$. The digital word sync signal is also available on this panel.

2.4 Gate Expander, Gate Drivers - Panel 4

An explanation of the Gate Expander, pulse stretching or overlap circuitry, will make use of the diagram of Figure 6. The delay properties of D type flip-flops is used to extend the width of each phase pulse by the down time of a single cycle of the MC.

In Figure 6 the ϕ_1 pulse is the input signal to the D_1 input and one input of the NOR gate. The other input to the NOR gate is Q_1 of the D_1 flip-flop.

The D_1 level is transferred to Q_1 only on the rise of the CK signal which in this case is the MC. The output of the NOR gate is low for any combination of inputs other than both being low. Both inputs will be low during the pulse interval that ϕ_1 is low, and the NOR gate output will be high.

Now consider that ϕ_1 rises. The output of the NOR gate drops beginning $\overline{\phi}_1(s)$. On the next rise of the MC, Q_1 will go high and remain high until the next rise of the MC occurs with D_1 low. D_1 goes low at the end of the ϕ_1 pulse, but Q_1 does not drop until the next rise of the MC. When this occurs both inputs of the NOR gate are low and the $\overline{\phi}_1(s)$ output is terminated, i.e. the output of the NOR gate goes from low to high. Thus, the $\overline{\phi}_1(s)$ pulse is a negative going pulse having a width of the original ϕ_1 pulse plus the down time of one cycle of the MC.

$\overline{\phi}_2(s)$ and $\overline{\phi}_3(s)$ are obtained in the same manner. Inversion by the phase driver amplifiers gives the proper phase for the CCD gates. Waveforms for $\overline{\phi}_1(s)$, $\overline{\phi}_2(s)$ and $\overline{\phi}_3(s)$ are shown in Figure 7.

Commercially available IC Clock Driver amplifiers, MH0026C, are used for the three phase pulses. The MH0026C is a dual amplifier with a common supply voltage input. Since three drivers are required two units are used resulting in one of the four amplifiers not being used.

Amplitude of the three phase outputs is controlled simultaneously by means of an active voltage source. This circuit is an emitter follower configuration which reduces the +30 volts to 0 - 20 volts by a single potentiometer. This control is on the front panel labelled PHASE LEVEL.

Initial off-set of each of the phase outputs is individually controlled by independent auxiliary biasing sources. These controls are referred to on the front panel as PHASE ADJUST.

The S and T output driver amplifiers are shown in Figure 7. The two amplifiers are idential and use an NPN and a PNP BJT in a noninverting complimentary configuration. Both type BJT's come four to a DIP package. The package diagram for each type device is shown in Figure 7. The terminal designations on the schematic correspond to the DIP package numbering.

2.5 Power Supply - Panel 5

Details of the supply voltage circuitry are shown in Figure 8. Input power requirements are nominally 115 volts at 60 Hz for each of the three self contained d-c supplies.

The dual supply is rated at 5 volts at 500 ma and $\pm$ 15 volts at 60 ma. The 30 volt supply is rated at 200 ma. The single 5 volt supply, used

for the DVM, is rated at 1 ampere.

Five LED's are used as panel indicators for the five d-c voltages. The 5 volt 1 ampere supply fuse is located behind the panel. The other two supplies have separate fuses located on the front panel.

3.0 IR DET IA AUX Unit

This auxiliary unit consists of three plug-in modules designated as panels 6, 7 and 8. Panel 6 contains a digital word generator for testing the CCD shift registers with an electronic signal input. Panel 7 is a DVM voltage monitoring circuit that also contains a reset pulse driver amplifier. The output of this amplifier replaces the charge lost by the source follower used for the output stage of the CCD shift register. Panel 8 is a variable bias supply used for controlling the voltage levels at eight different points in the CCD control circuitry.

3.1 Digital Word Generator - Panel 6

The digital word generator output is a series of pulses. The number of pulses determines the word length which is controlled by the Word Length switch on the front panel. This switch is labelled 2^0 through 2^5 for word lengths corresponding to 1, 2, 4, 8, 16 and 32 pulses respectively.

The time interval between the start of one word and the initiation of the next word is referred to as the word period. This interval is specified in terms of the number of pulses that could occur for a particular word period. The Word Period switch on the front panel is labelled 2^6 through 2^{11} for word periods of 64, 128, 256, 512, 1024 and 2048 pulses respectively.

The Word Period and the Word Length controls are independent of each other. As an example, let the Word Length switch be set to 2^3 and the

Word Period switch be set to 2^7. The output of the word generator would be 8 pulses followed by no pulses for an interval corresponding to 120 additional pulse intervals. See Figure 17 which is a photograph of the output of the word generator for the given conditions of this example.

A working diagram of the Word Generator circuit is shown in Figure 9. The output pulses from gate A_3 are generated by two monostable flip-flops, SN74123, connected in cascade. The first flip-flop output, the input to the second flip-flop, is delayed by the variable RC time constant labelled DELAY on the front panel. The final output pulse width is controlled by the variable RC time constant of the second flip-flop labelled on the front panel as WIDTH.

The final output of the word generator has a controlled off-set as well as a variable amplitude. The off-set is adjustable from 0 to 4 volts by means of the front panel control called BIAS. The amplitude of the output word is variable from 0 to 3 volts by means of the front panel control called LEVEL.

Input pulses to the first monostable flip-flop are controlled by a two input NAND gate. One input to this NAND gate, A_2, is a constant pulse train having the frequency of either the internal Master Clock or an external Clock signal. The other input to the control NAND gate is the Q output of a D-type flip-flop, SN7474. An input to the first monostable flip-flop is determined by the proper coincidence of the two inputs to the controlled NAND gate, A_2.

The logic level of the Q output of the D-type flip-flop is controlled by the Clear and Preset levels. When the Clear input goes low, or to a 0 logic level, the Q level will go to a 0 logic level. When the Preset input goes low the Q output level will go high, or a 1 logic level.

The Clear signal is controlled by the outputs of a ripple counter. As indicated in Figure 9 the ripple counter consists of 12 four-bit binary counters connected in cascade, (SN7493). The input to the first counter is the same constant pulse train used as one input to A_2. The outputs of the first six counters correspond to the Word Length switch positions 2^0 through 2^5. The Preset signal is controlled by the outputs of the last six counters by means of the Word Period switch positions 2^6 through 2^{11}.

The Reset inputs to all counters are tied together with a common connection to the pole of the Word Period switch and one input to the NAND gate A_4 which controls the Preset signal. When the Reset signal goes high all counters are reset to a 0 output logic level and the Preset signal, the output of A_4, also goes low resulting in Q of the D-type flip-flop going high.

Assume that at time t_o all counters have been reset to a 0 logic level, the Word Length switch set to 2^3 and the Word Period switch set to 2^6. Resetting the counters to a 0 logic level has left Q of the D-type flip-flop in the high state. The A_2 gate will now trigger the first monostable flip-flop and the word generator output will be a pulse for the first 8 inputs to the counter. The 8th input will result in the output of the 4th counter going high. The Clear signal at the output of the NAND gate B_1 will go low. This will put the Q output of the D-type flip-flop at a low level and deactivate the A_2 NAND gate, thereby giving no further output from the word generator. On the 64th input to the first counter the output of the 7th counter will go high. All counters are reset to a 0 level, Preset goes low, Q output goes high and the sequence begins anew.

3.2 DVM Monitor and Reset Pulse - Panel 7

The input to the DVM may be connected directly to the EXT VOLT jacks on the front panel - VOLTAGE SELECTOR switch set to EXT - or switched to 10 hard wired monitor points. The actual DVm input can only take positive voltages not exceeding +1.99 volts. An internal attenuator is used to rescale the meter indication to +19.9 volts full scale.

Two of the hard wired monitor points are negative voltages. Inverting circuitry is used at each of these points so that the actual monitored voltage is positive as required by the DVM. On the front panel on either side of the DVM is an LED. On the left side the LED is marked -. On the right side the LED is marked +. These LED's indicate the actual polarity of the original monitored voltage.

The setting of the VOLTAGE SELECTOR switch is indicated by an LED located adjacent to the control knob for each of the 10 hard wired monitor points. Eight of these are located on Panel 8, one on Panel 7 and one on Panel 4 of the IRDSS.

Circuit details of the DVM monitor panel are shown in Figure 10. Figure 10 also indicates the circuit details of the reset pulse amplifier. The driver amplifier is the same as that used for the three phase drivers with the exception that no provision is made for an off-set voltage. The amplitude is variable from 0 to 20 volts.

As indicated in Figure 10 the pulse width of the reset pulse is determined by the coincidence of the inputs to a two input NAND gate. One of these inputs is ϕ_2 and the other ϕ_1'. Both of these inputs are obtained from the Pulse Stretcher and Gate Driving Amplifier module, or Panel 4. ϕ_1' is the Q output from the ϕ_1 D-type flip-flop. With these two signals the

reset pulse width is equal to the amount that the origianl phase pulse is stretched, i.e., the difference between ϕ_1 and $\phi_1(s)$.

3.3 Bias Control - Panel 8

Circuit details of the bias control panel are shown in Figure 11. Five emitter followers provide voltage sources variable from 0 to 20 volts. One source provides 0 to 10 volts with a vernier control from 0 to 5 volts. One negative provides 0 to -5 volts and another 0 to -10 volts. The two negative sources are monitored by means of unity gain inverters as indicated in Figure 11.

4.0 Operation and Evaluation

Waveforms at the various test points of this electronic system are shown in Figures 12 through 19. Figure 20 is the output for a CCD unit with a digital word of four bits as the input signal to the shift register.

Evaluation is continuing although certain modifications already appear desirable. One of these is some control over the fall time of the clock pulses which for the present model appear to be too short for optimum operation. This appears necessary for the particular structures being investigated, however, for other type CCD's the sharp waveforms of this prototype may be more desirable. An improved master clock with better control of the duty cycle is being investigated. Additional modifications may become evident with further evaluation.

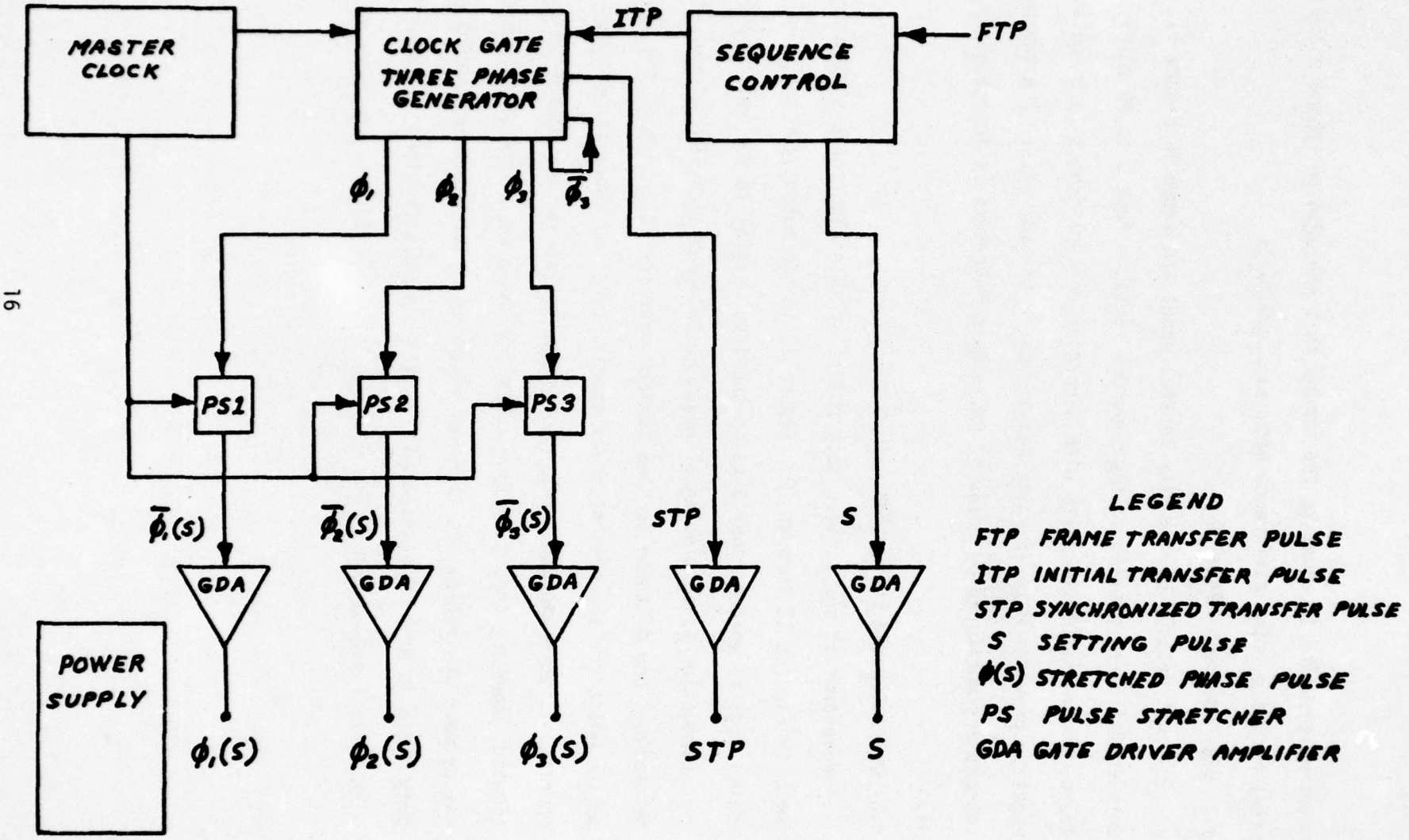


Figure 1. Block diagram of IRDSS Model I

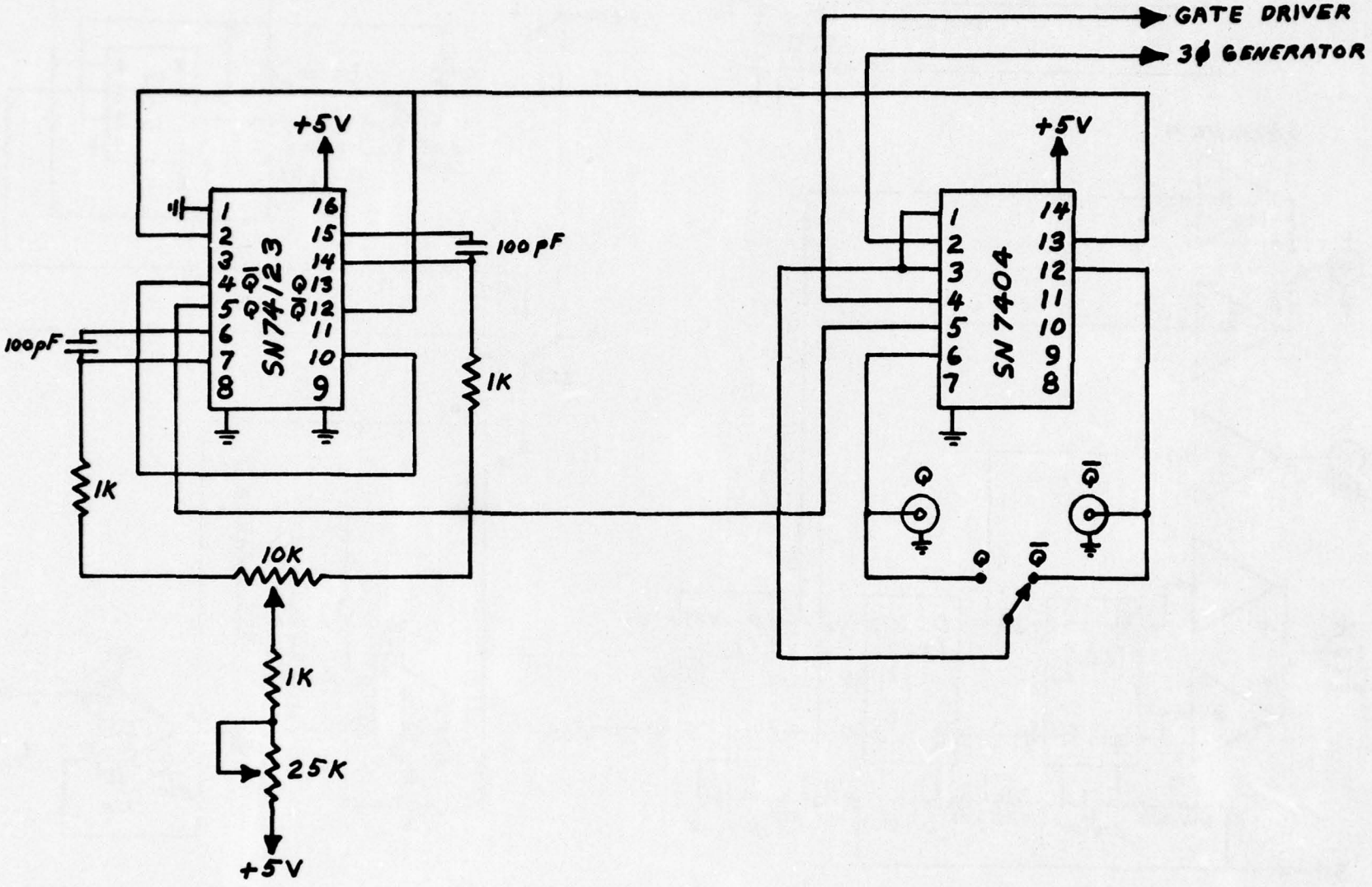


Figure 2. Master Clock Circuitry

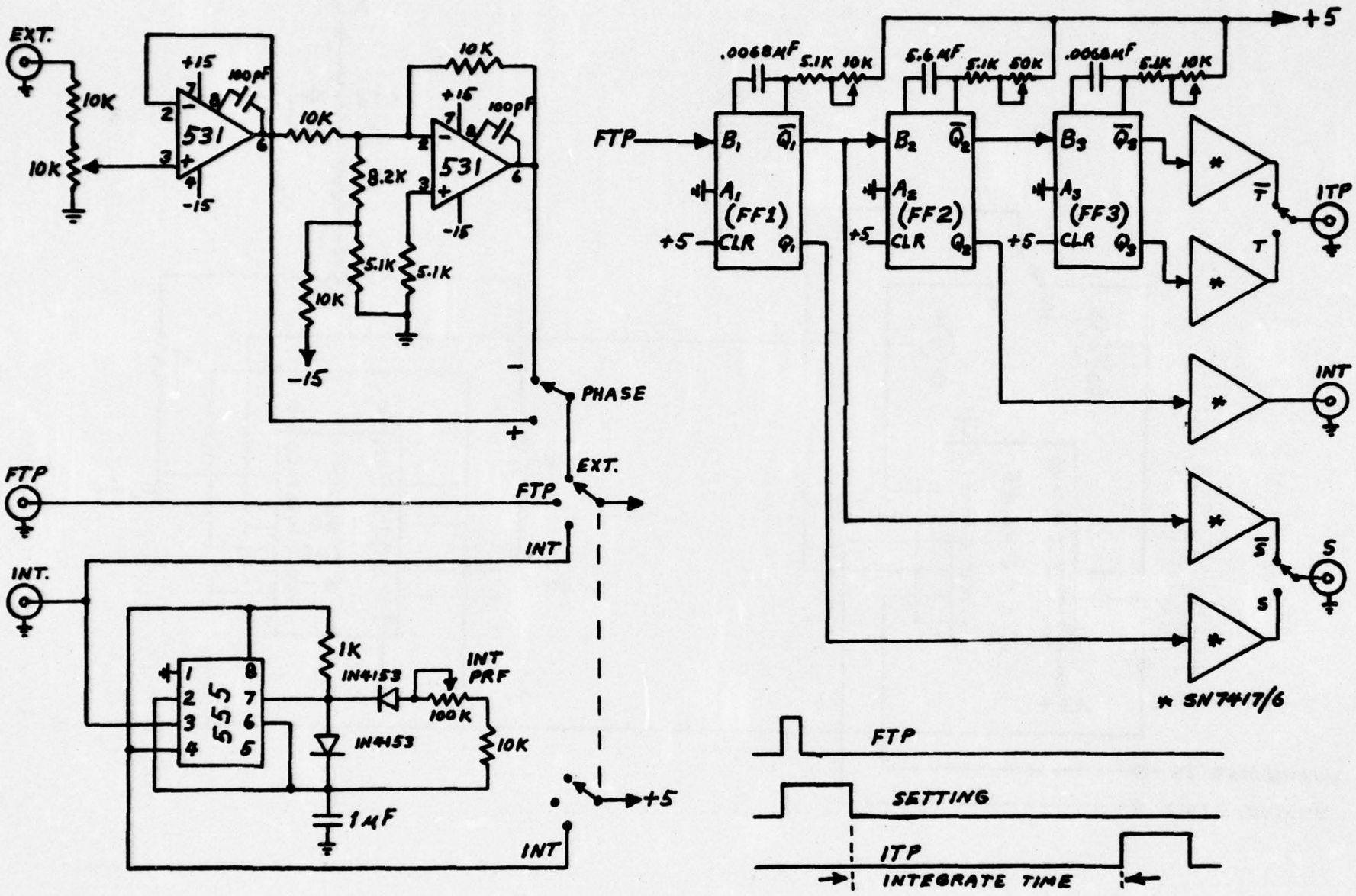


Figure 3. Sequence Control Circuitry

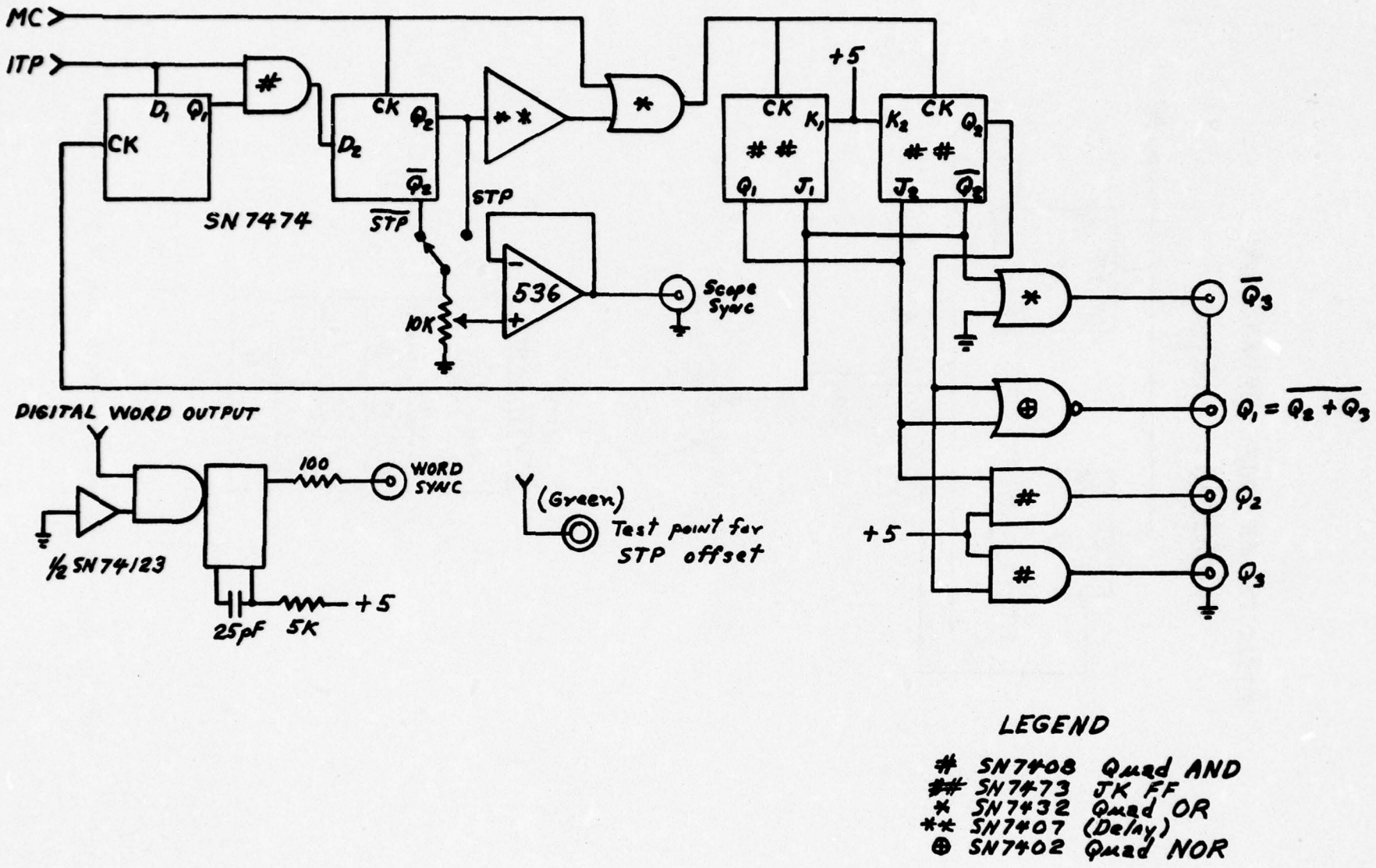
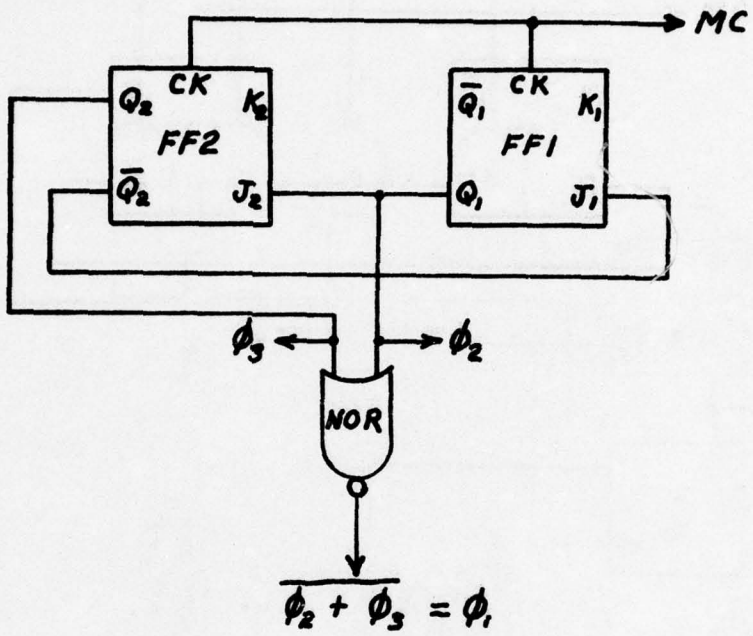


Figure 4. Clock Gate, Three Phase Generator circuitry

BASIC THREE PHASE GENERATOR



J-K
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

Figure 5. Basic three phase generator and JK truth table.

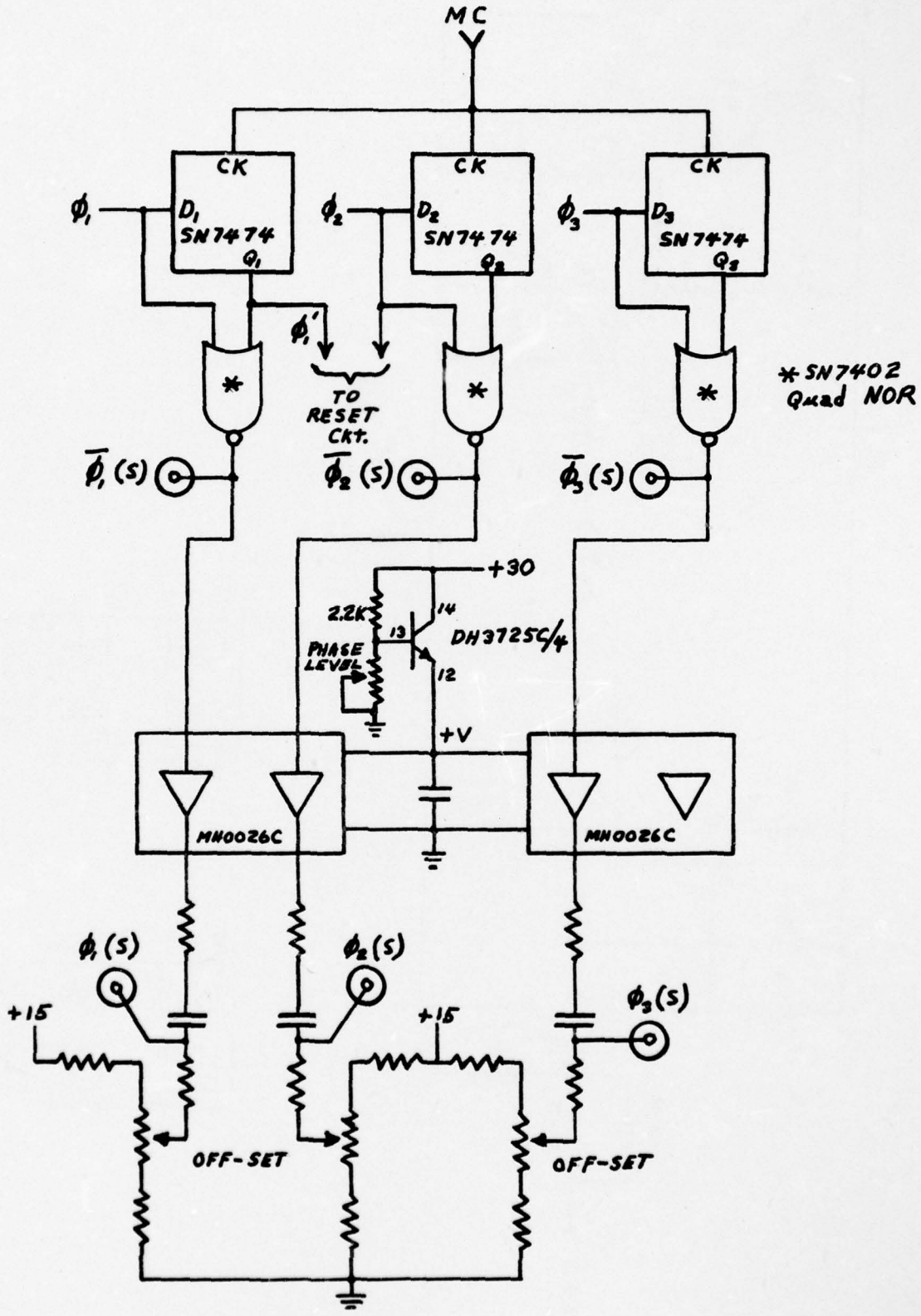
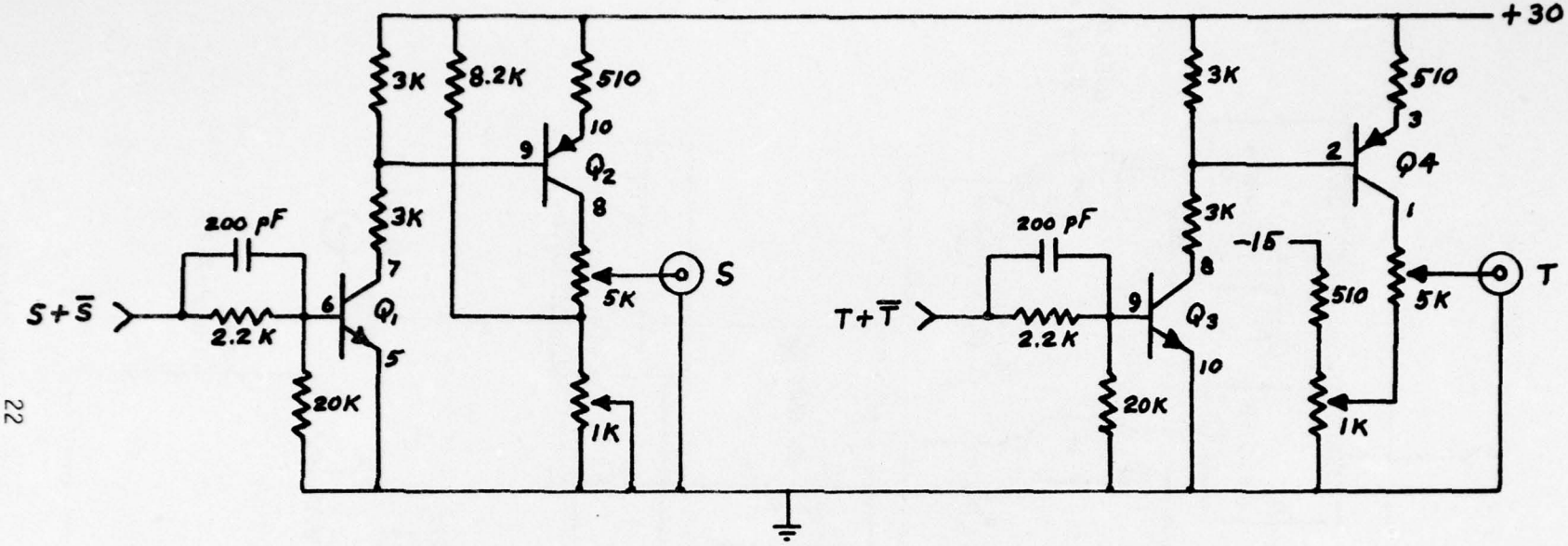
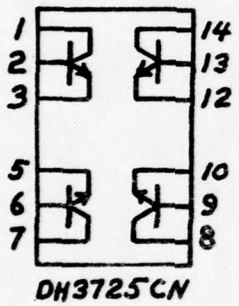


Figure 6. Gate Expander, Gate Driver circuitry





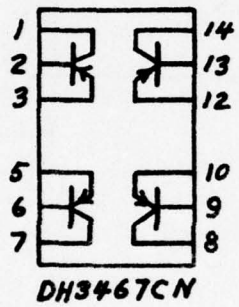


Figure 7. Setting and Transfer driver amplifiers

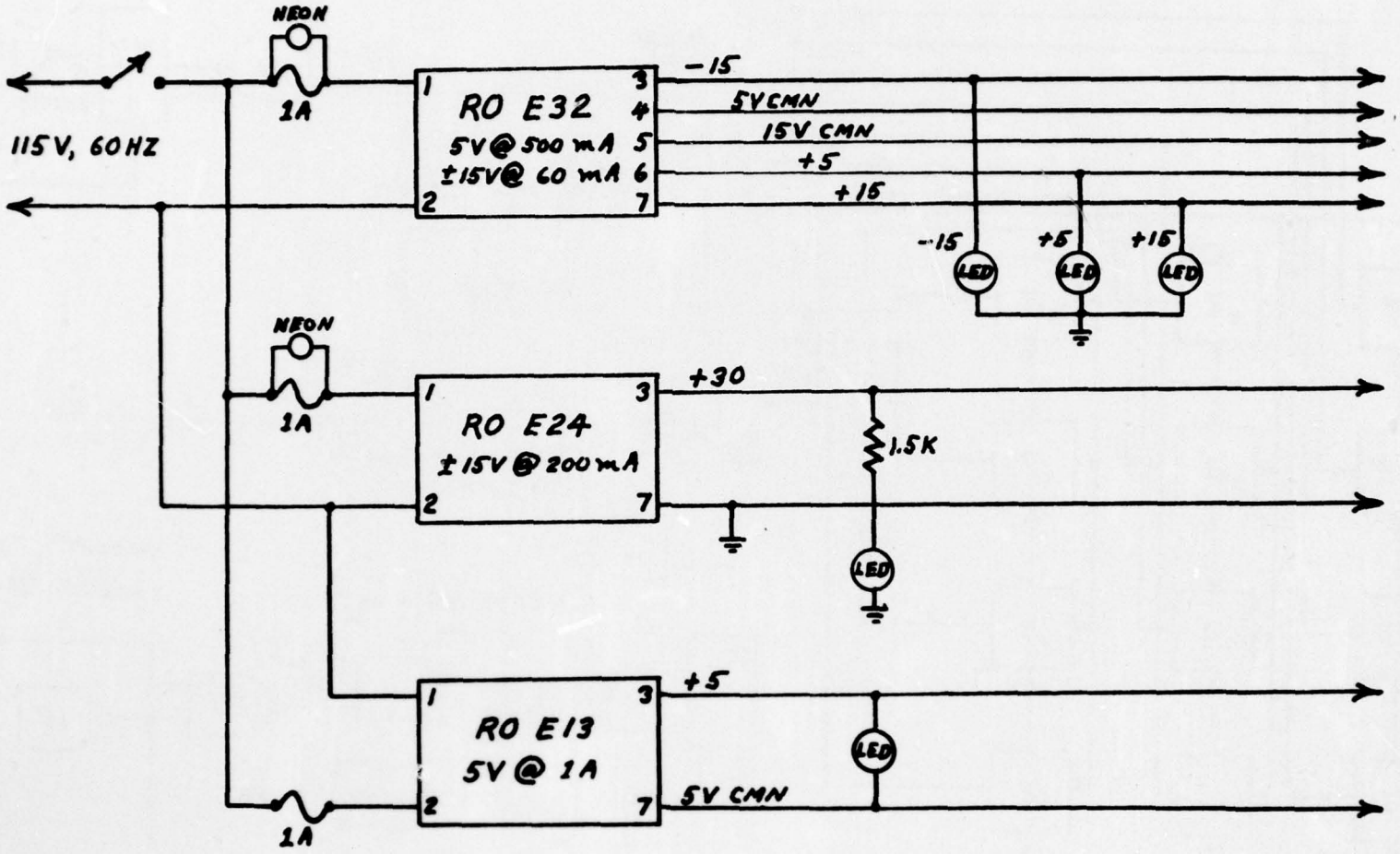


Figure 8. Power Supply circuitry

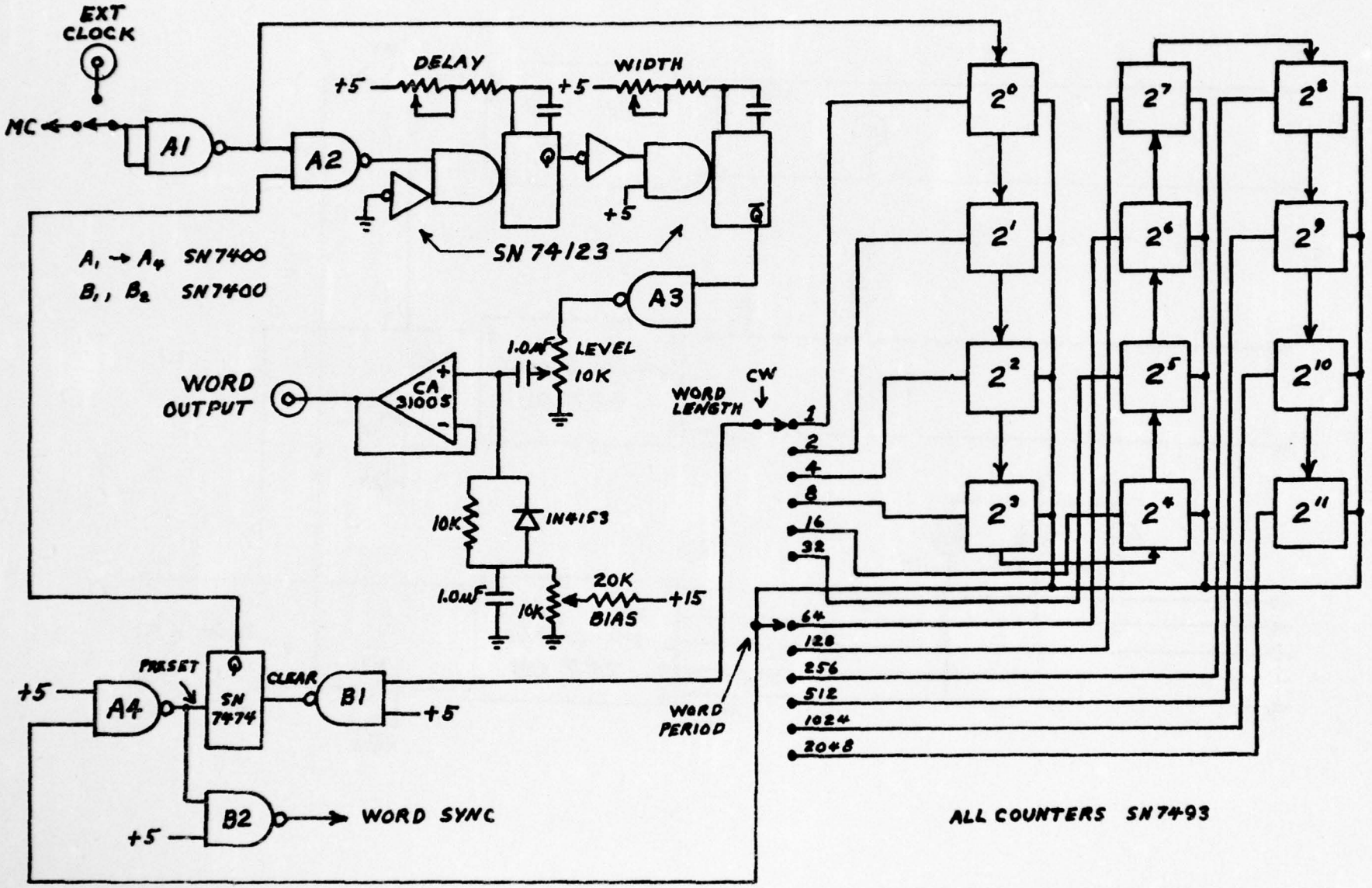


Figure 9. Digital word generator circuitry

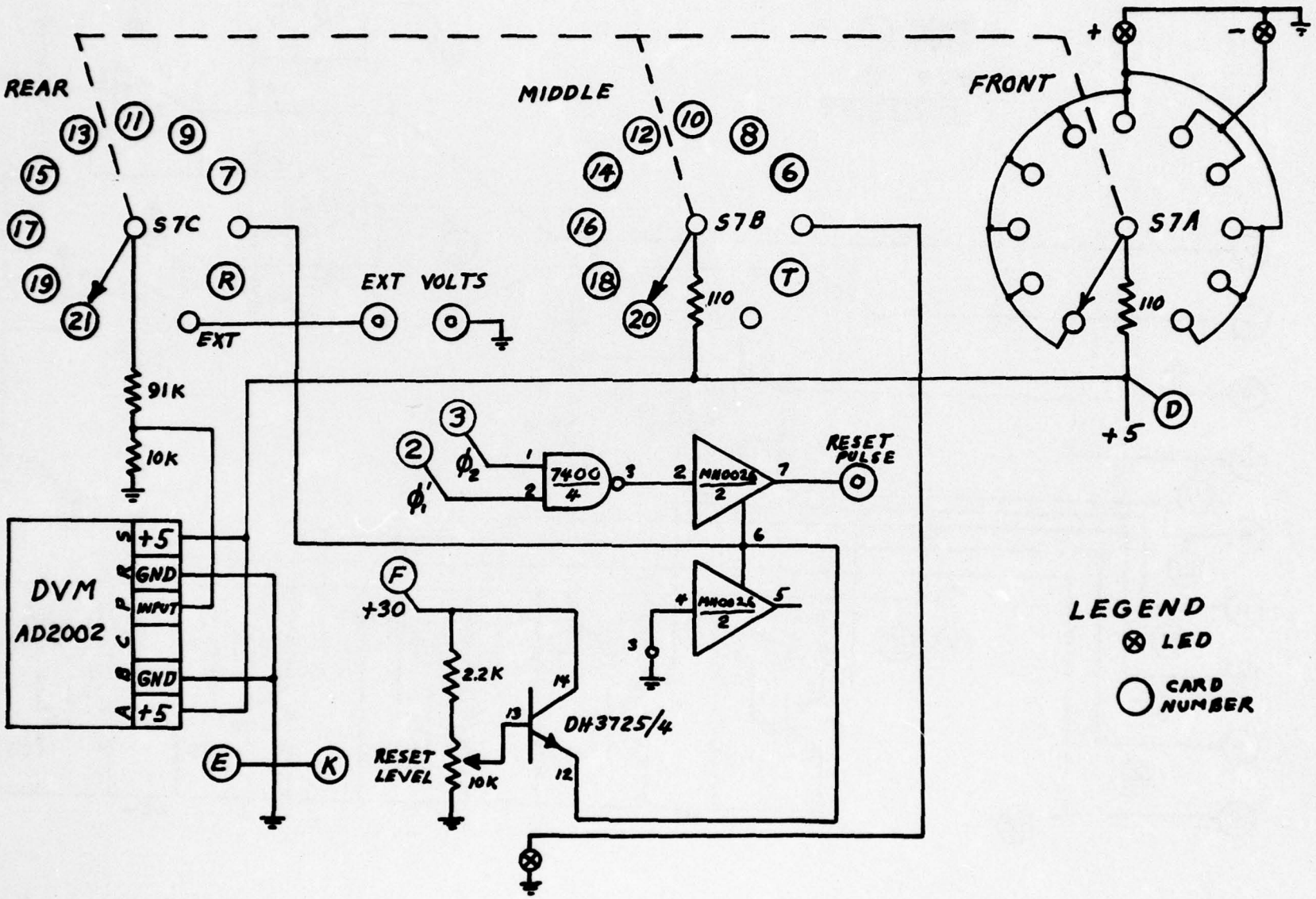


Figure 10. DVM Monitor and Reset Pulse circuitry

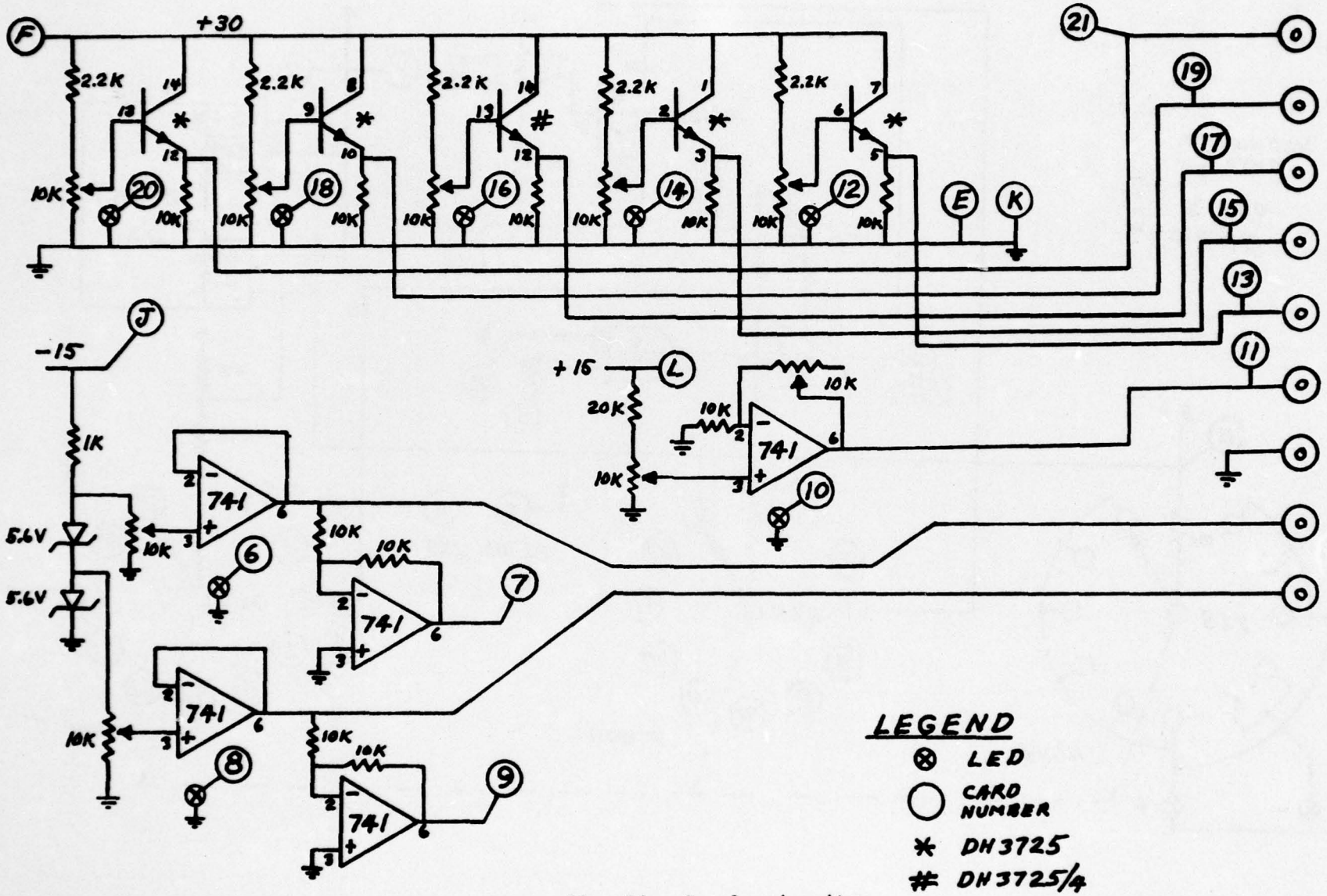
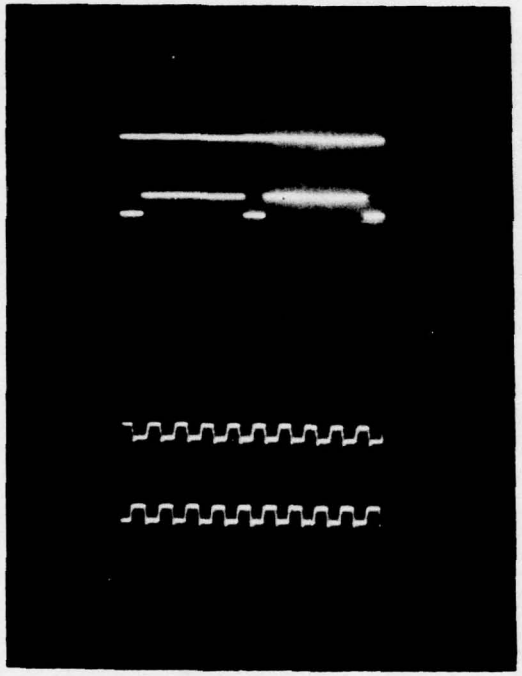


Figure 11. Bias Supply circuitry



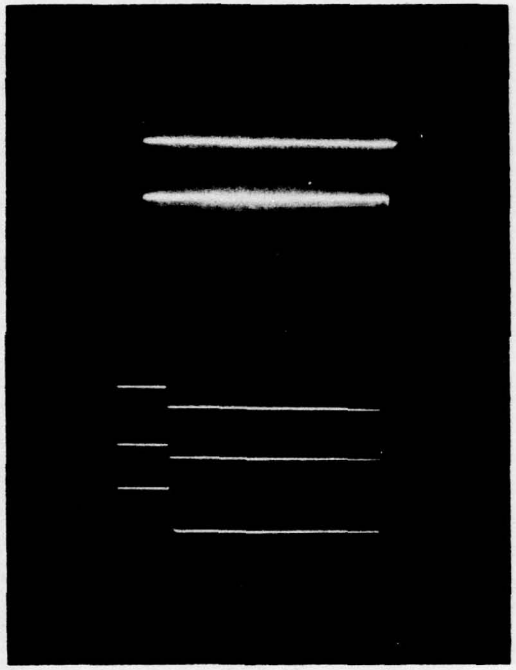
Setting pulse

Integrate time

5 Volts/div, 5 msec/div

Master Clock $\frac{\phi}{\phi}$ 5 Volts/div, 1 μsec/div

Figure 12. Setting, Integrate and Master Clock waveforms



Setting Pulse

5 Volts/div, 2 msec/div

ITP Pulse

ITP Pulse

GDTP Pulse

5 Volts/div, 10 μsec/div

STP Pulse

Figure 13. Setting and ITP pulses separated by the integration time, ITP, GDTP and STP pulses

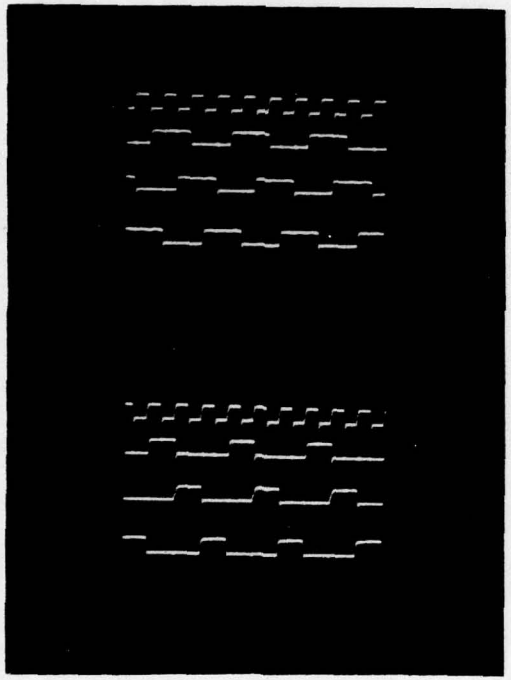
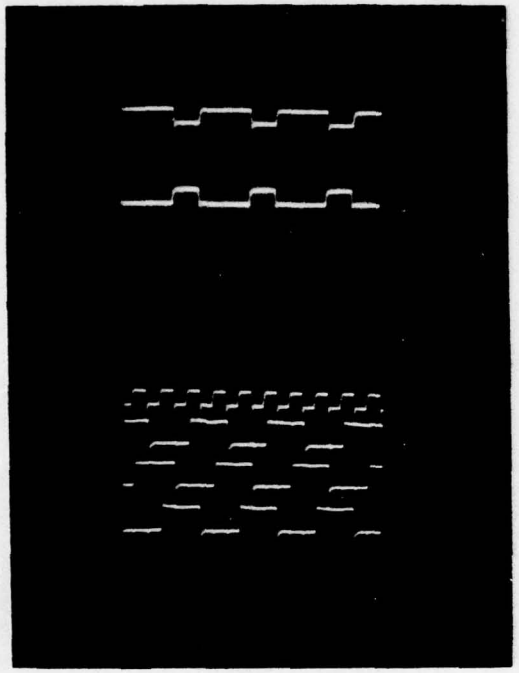


Figure 14. Master Clock, stretched complemented three phase and initial three phase waveforms



$\bar{\phi}_3$

ϕ_3

5 Volts/div, 1 μsec/div

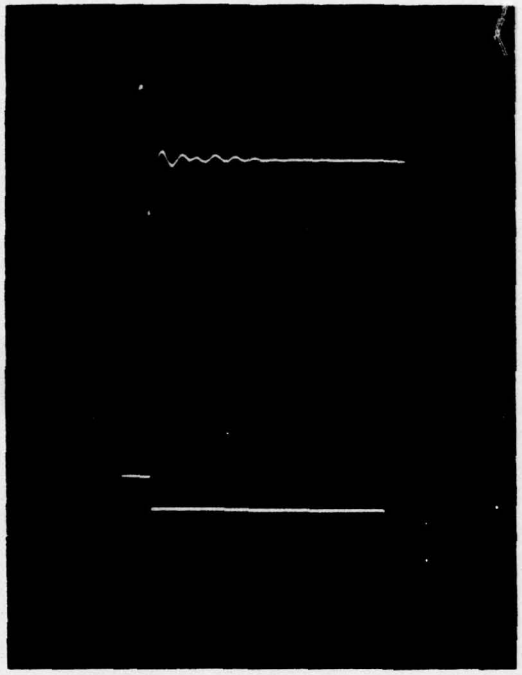
Master Clock

$\phi_1(s)$

$\phi_2(s)$

$\phi_3(s)$

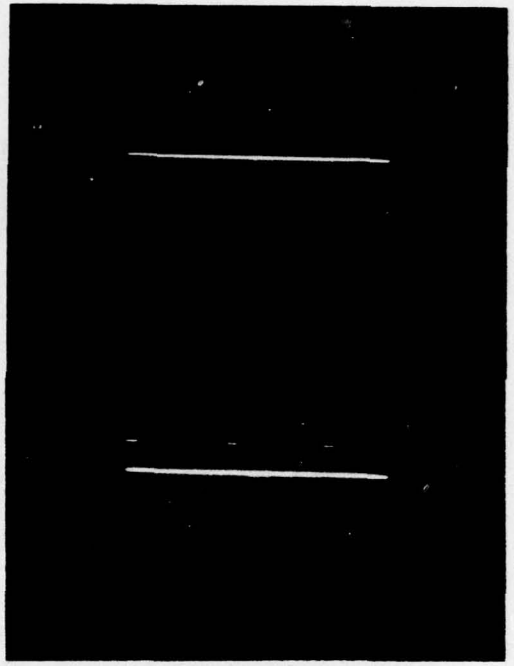
Figure 15. Phase three complement, phase three, Master Clock and the three phase stretched pulse waveforms



Digital word sync 1 Volt/div, 0.1 μsec/div

Scope sync (STP) 1 Volt/div, 20 μsec/div

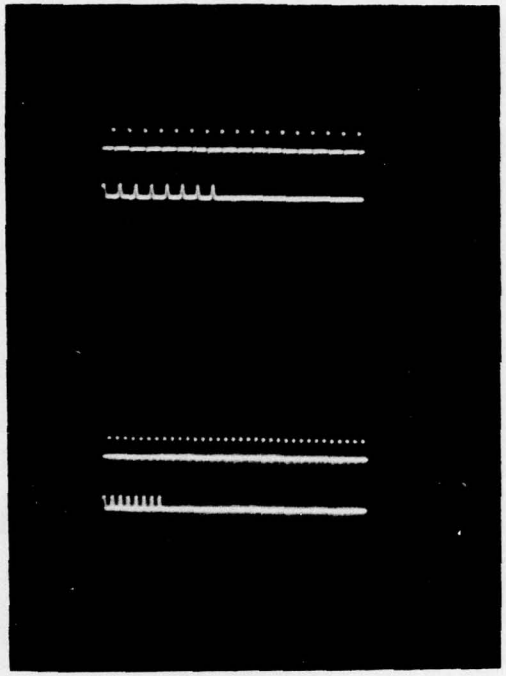
Figure 16. Digital word and Scope (STP) sync waveforms



2 Volts/div, greater than 20 μsec/div

2 Volts/div, 50 μsec/div

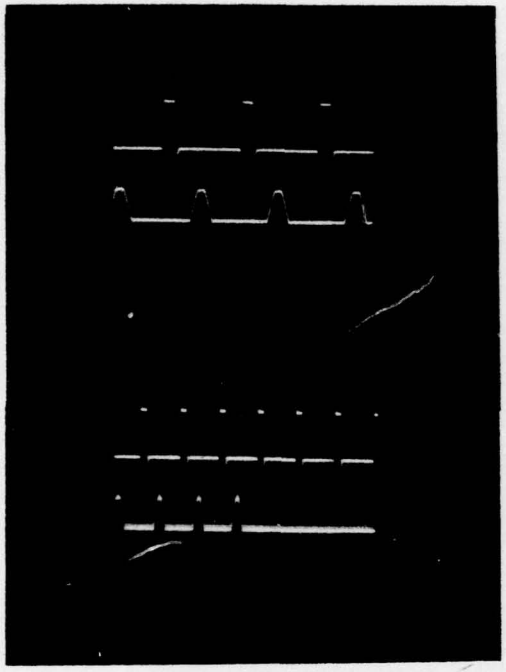
Figure 17. Digital Word Generator Output for 8 bit word and 64 bit period.



5 Volts/div, 10 μsec/div

5 Volts/div, 5 μsec/div

Figure 18. Reset pulse and 8 bit word waveforms



Reset Pulse

2 Volts/div, 1 μsec/div

4 bit word

Reset Pulse

2 Volts/div, 2 μsec/div

4 bit word

Figure 19. Reset Pulse and 4 bit word waveforms

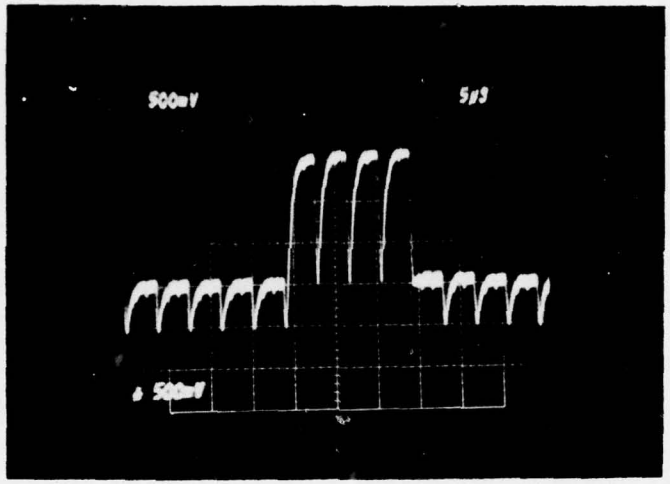


Figure 20. CCD output for a four bit word input

PERSONNEL

A list of the scientists and engineers who contributed to the work reported is given below:

B. L. Cochrun, Professor of Electrical Engineering
Principal Investigator

J. Blacquier, Technician

R. Aylward, Graduate Student

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